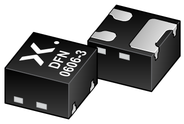

PMH550UNEA

30 V, N-channel Trench MOSFET

11 July 2024

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN0606-3 (SOT8001) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM
- Leadless ultra small and ultra thin SMD plastic package: 0.62 x 0.62 x 0.37 mm
- AEC-Q101 qualified

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	-	30	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	-	770	mA
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 770 mA; T_j = 25 °C		-	550	670	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2.

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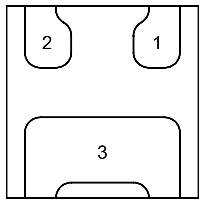
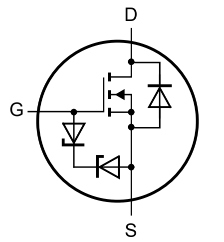
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view **DFN0606-3 (SOT8001)**	
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMH550UNEA	DFN0606-3	plastic, leadless ultra small package; 3 terminals; body 0.62 x 0.62 x 0.37 mm	SOT8001

7. Marking

Table 4. Marking codes

Type number	Marking code
PMH550UNEA	`0011` `0111`

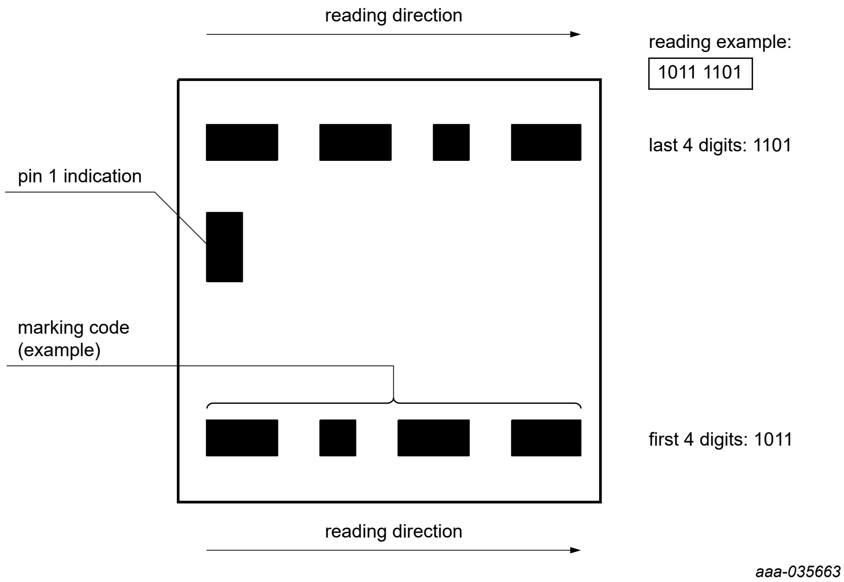


Fig. 1. DFN0606-3 (SOT8001) binary marking code description

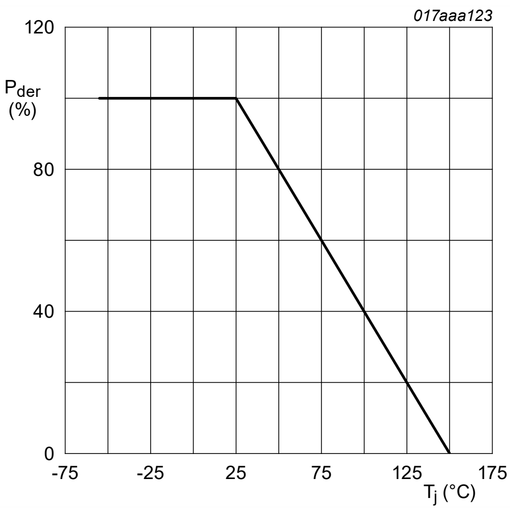
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

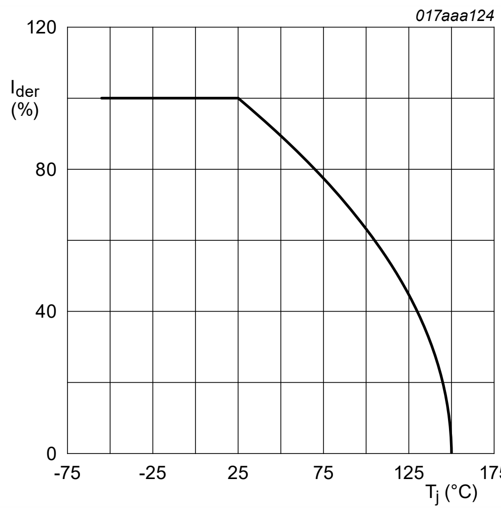
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T_j = 25 °C		-	30	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	V_{GS} = 4.5 V; T_{amb} = 25 °C	[1]	-	770	mA
		V_{GS} = 4.5 V; T_{amb} = 100 °C	[1]	-	485	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; single pulse; t_p ≤ 10 µs		-	3	A
P_{tot}	total power dissipation	T_{amb} = 25 °C	[2]	-	380	mW
			[1]	-	710	mW
		T_{sp} = 25 °C		-	2.8	W
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	T_{amb} = 25 °C	[1]	-	680	mA
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[3]	-	2000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 1 cm^2.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[3] Measured between all pins.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig. 2. Normalized total power dissipation as a function of junction temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig. 3. Normalized continuous drain current as a function of junction temperature

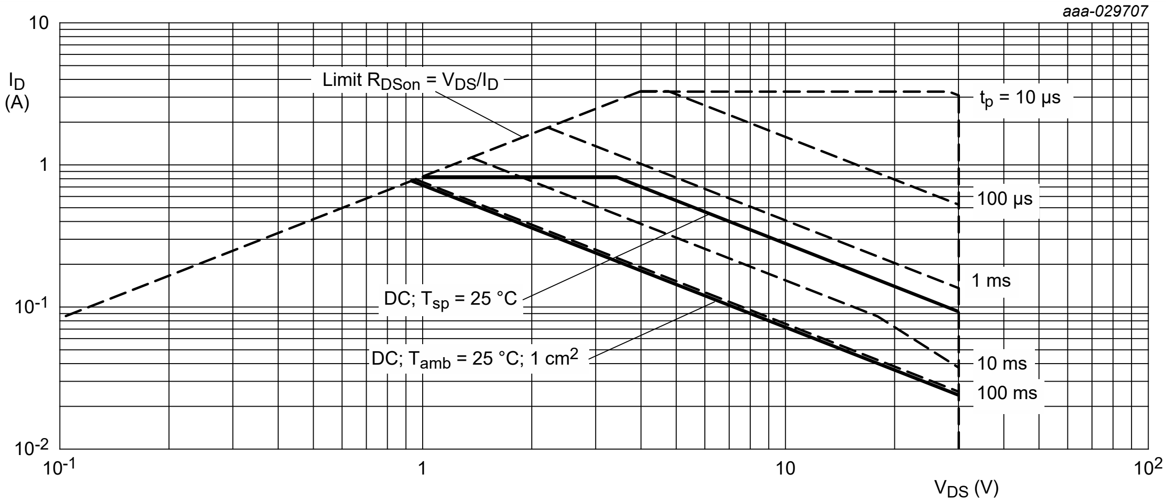


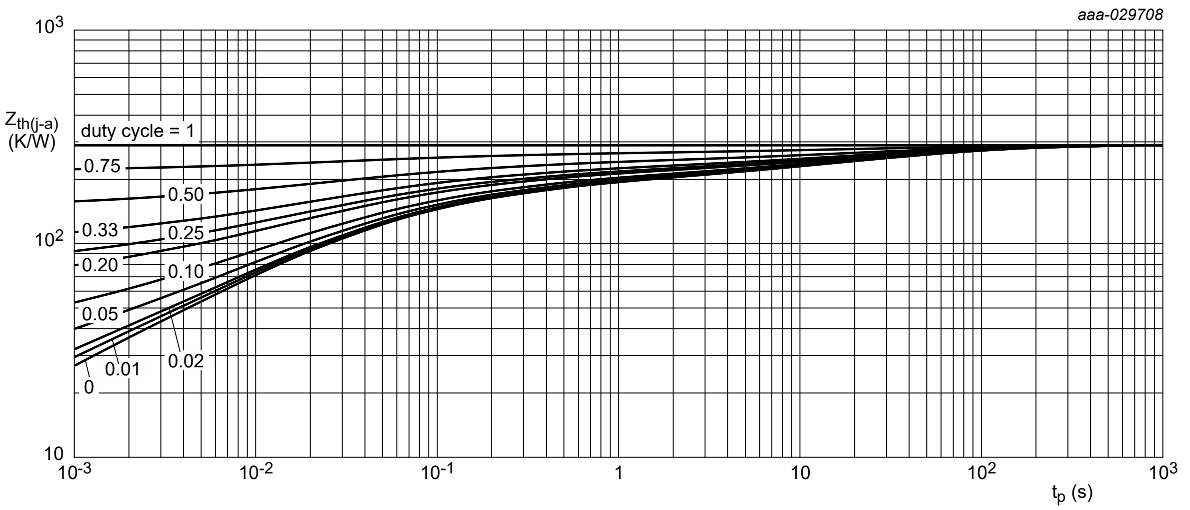
Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

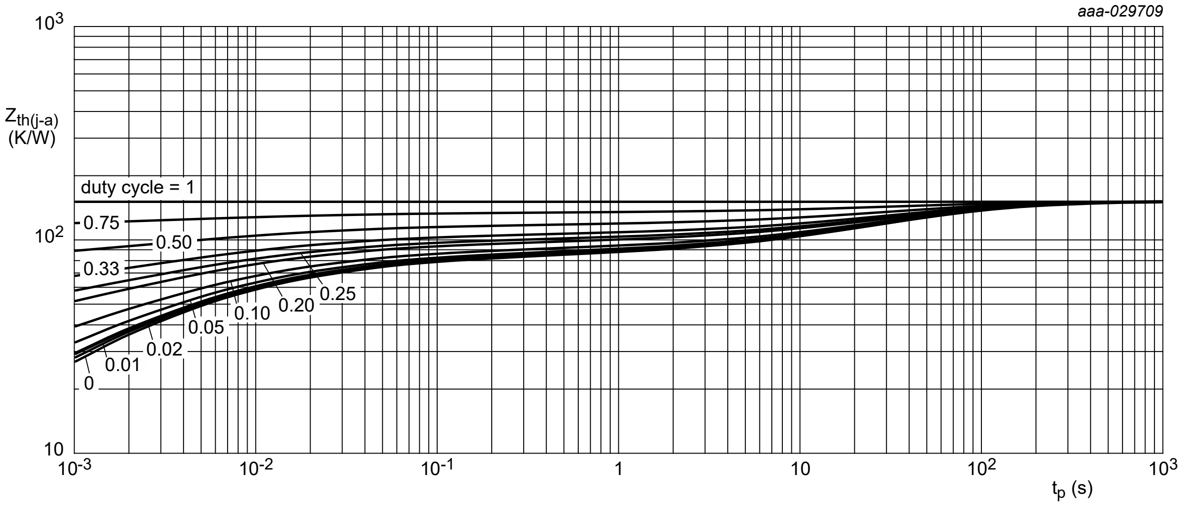
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	285	330	K/W
			[2]	-	150	175	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	38	45	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm^2.



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



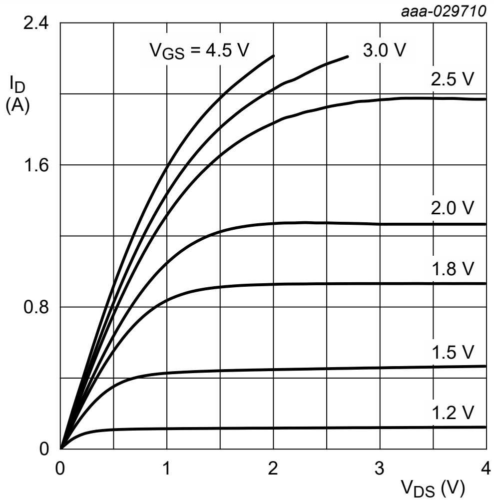
FR4 PCB, mounting pad for drain 1 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

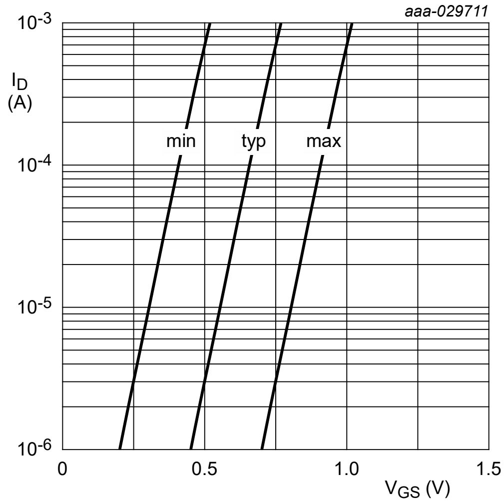
Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		30	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 250 µA; V_{DS} = V_{GS}; T_j = 25 °C		0.45	0.7	0.95	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 °C		-	-	1	µA
I_{GSS}	gate leakage current	V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	5	µA
		V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-5	µA
		V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	1	µA
		V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-1	µA
		V_{GS} = 2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	100	nA
		V_{GS} = -2.5 V; V_{DS} = 0 V; T_j = 25 °C		-	-	-100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 770 mA; T_j = 25 °C		-	550	670	mΩ
		V_{GS} = 4.5 V; I_D = 770 mA; T_j = 150 °C		-	990	1200	mΩ
		V_{GS} = 2.5 V; I_D = 770 mA; T_j = 25 °C		-	660	900	mΩ
		V_{GS} = 1.8 V; I_D = 80 mA; T_j = 25 °C		-	770	1120	mΩ
		V_{GS} = 1.5 V; I_D = 10 mA; T_j = 25 °C		-	890	1500	mΩ
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 770 mA; T_j = 25 °C		-	2.2	-	S
R_G	gate resistance	f = 1 MHz		-	19	-	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	V_{DS} = 15 V; I_D = 770 mA; V_{GS} = 4 V; T_j = 25 °C		-	0.38	0.4	nC
Q_{GS}	gate-source charge			-	0.1	-	nC
Q_{GD}	gate-drain charge			-	0.1	-	nC
C_{iss}	input capacitance	V_{DS} = 15 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25 °C		-	30.3	-	pF
C_{oss}	output capacitance			-	5.1	-	pF
C_{rss}	reverse transfer capacitance			-	3.7	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; I_D = 770 mA; V_{GS} = 4 V; $R_{G(ext)}$ = 6 Ω; T_j = 25 °C		-	1	-	ns
t_r	rise time			-	2	-	ns
$t_{d(off)}$	turn-off delay time			-	4	-	ns
t_f	fall time			-	2	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 680 mA; V_{GS} = 0 V; T_j = 25 °C		-	0.9	1.2	V



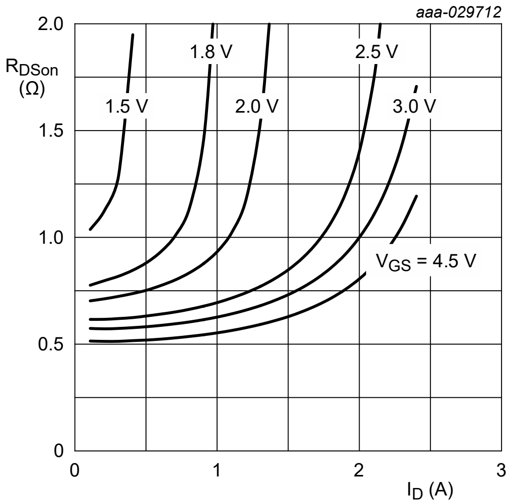
T_j = 25 °C

Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values



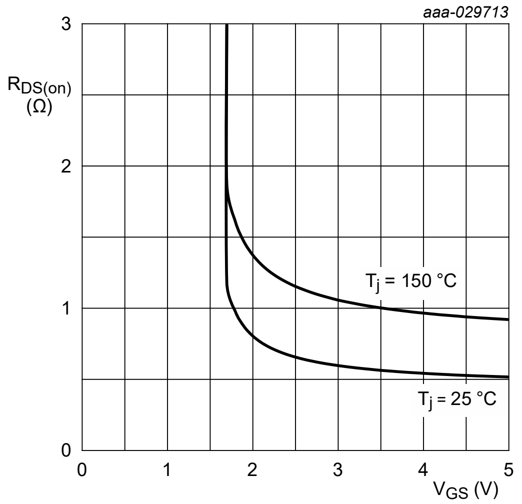
T_j = 25 °C; V_{DS} = 5 V

Fig. 8. Sub-threshold drain current as a function of gate-source voltage



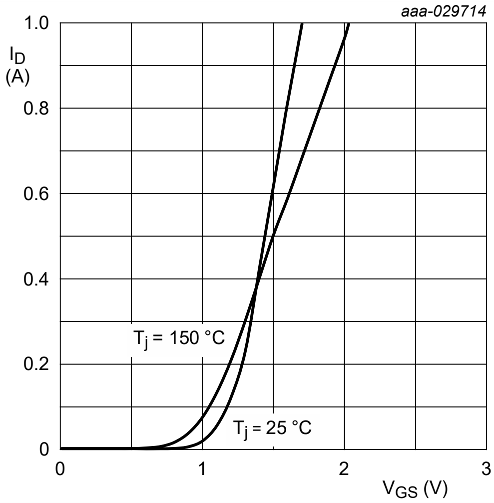
T_j = 25 °C

Fig. 9. Drain-source on-state resistance as a function of drain current; typical values



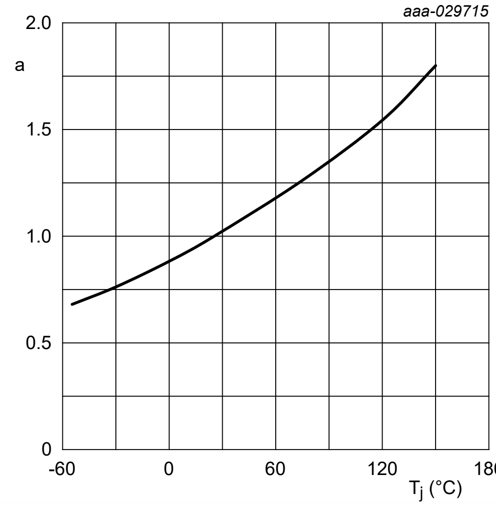
I_D = 0.6 A

Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



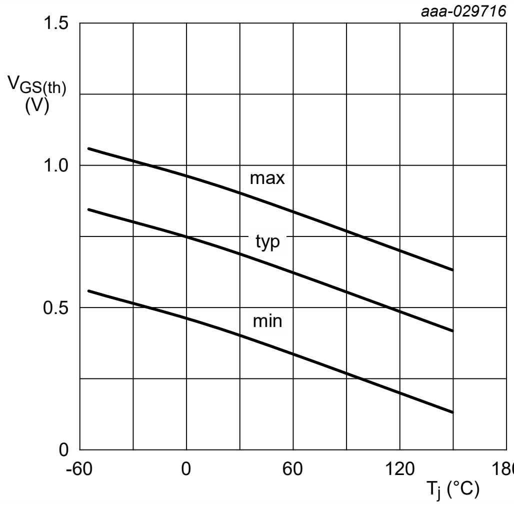
$V_{DS} > I_D \times R_{DSon}$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values



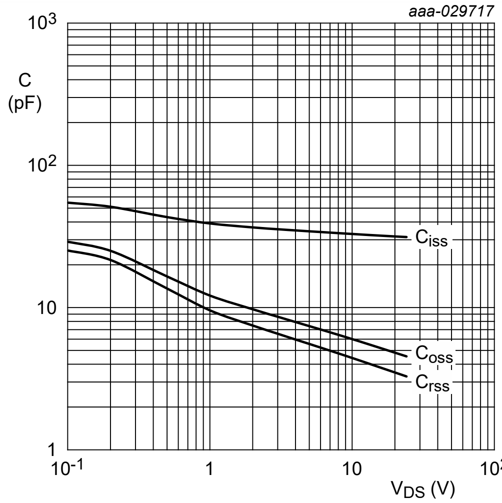
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values



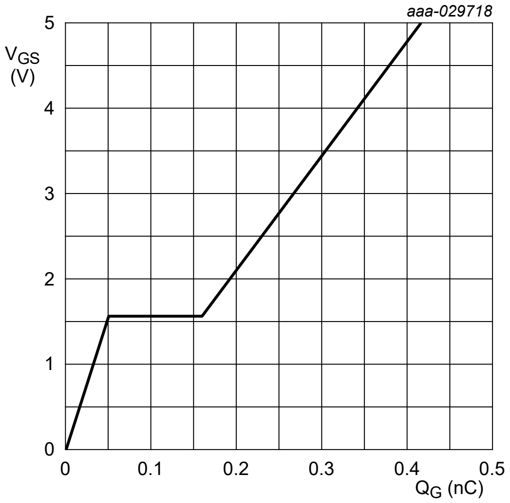
I_D = 250 µA; $V_{DS} = V_{GS}$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



f = 1 MHz; V_{GS} = 0 V

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



I_D = 0.6 A; V_{DS} = 15 V; T_{amb} = 25 °C

Fig. 15. Gate-source voltage as a function of gate charge; typical values

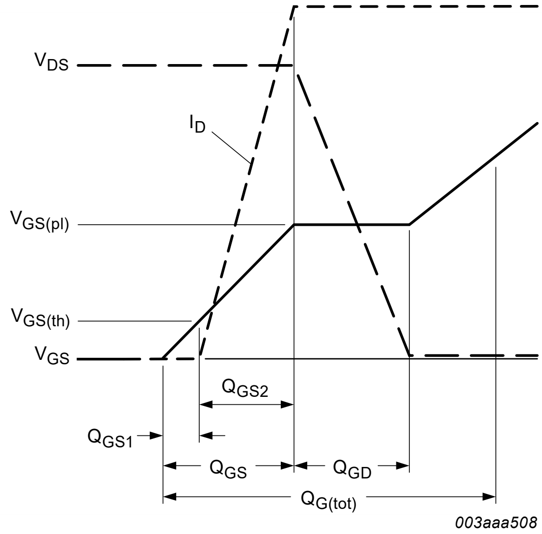
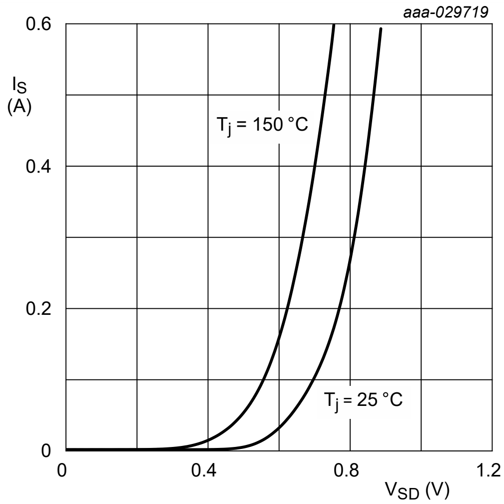


Fig. 16. Gate charge waveform definitions



V_{GS} = 0 V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

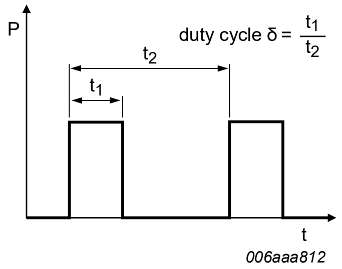


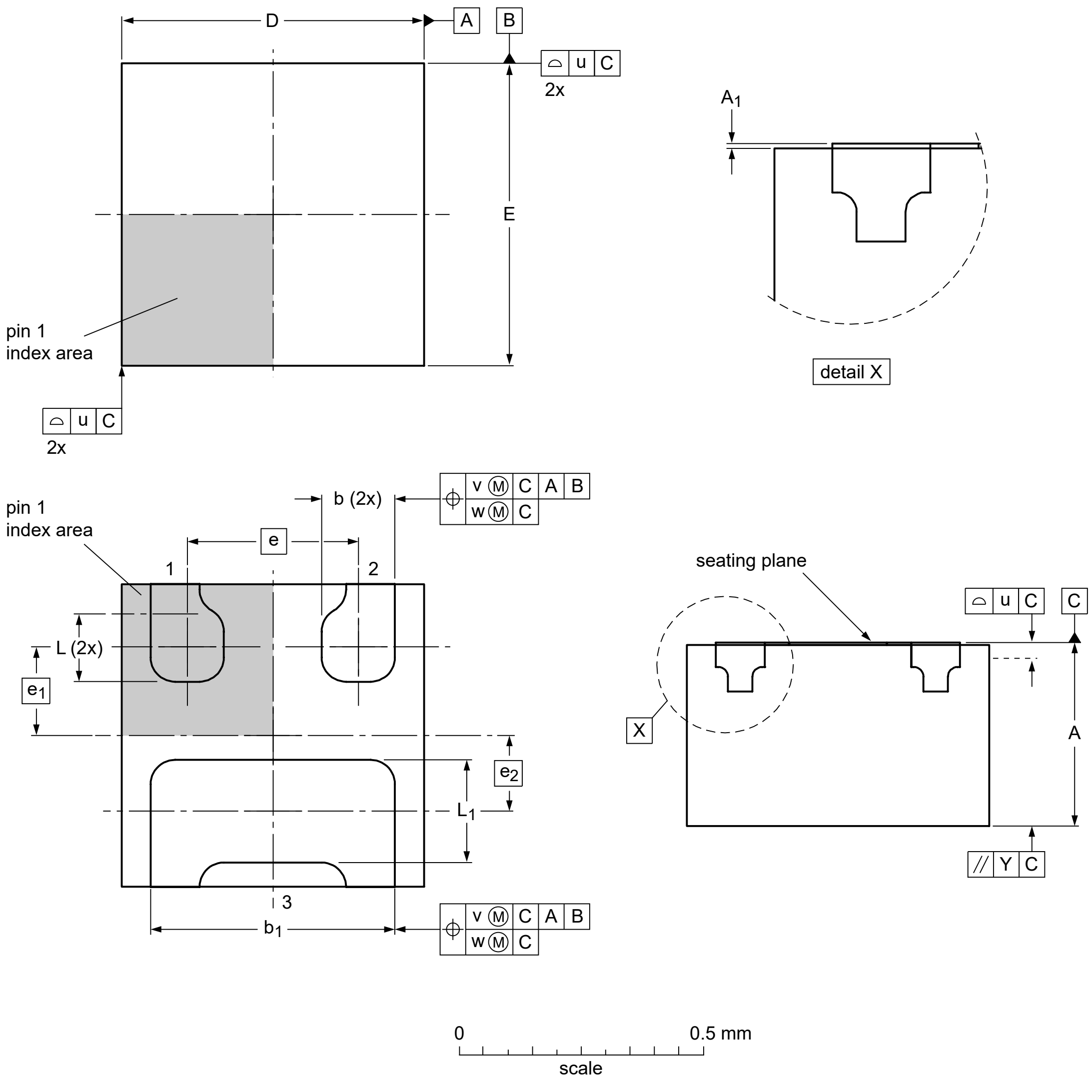
Fig. 18. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN0606-3, plastic, leadless ultra small package; 3 terminals; body 0.62 x 0.62 x 0.37 mm **SOT8001**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_1	D	E	e	e_1	e_2	L	L_1	u	v	w	Y
	max	0.40	0.04	0.20	0.55						0.20	0.26				
mm	nom	0.37		0.15	0.50	0.62	0.62	0.35	0.186	0.155	0.15	0.21	0.05	0.1	0.05	0.05
	min	0.34		0.10	0.45						0.10	0.16				

sot8001_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8001		- - -				~~18-12-03~~ 18-12-05

Fig. 19. Package outline DFN0606-3 (SOT8001)

13. Soldering

Footprint information for reflow soldering of DFN0606-3 package **SOT8001**

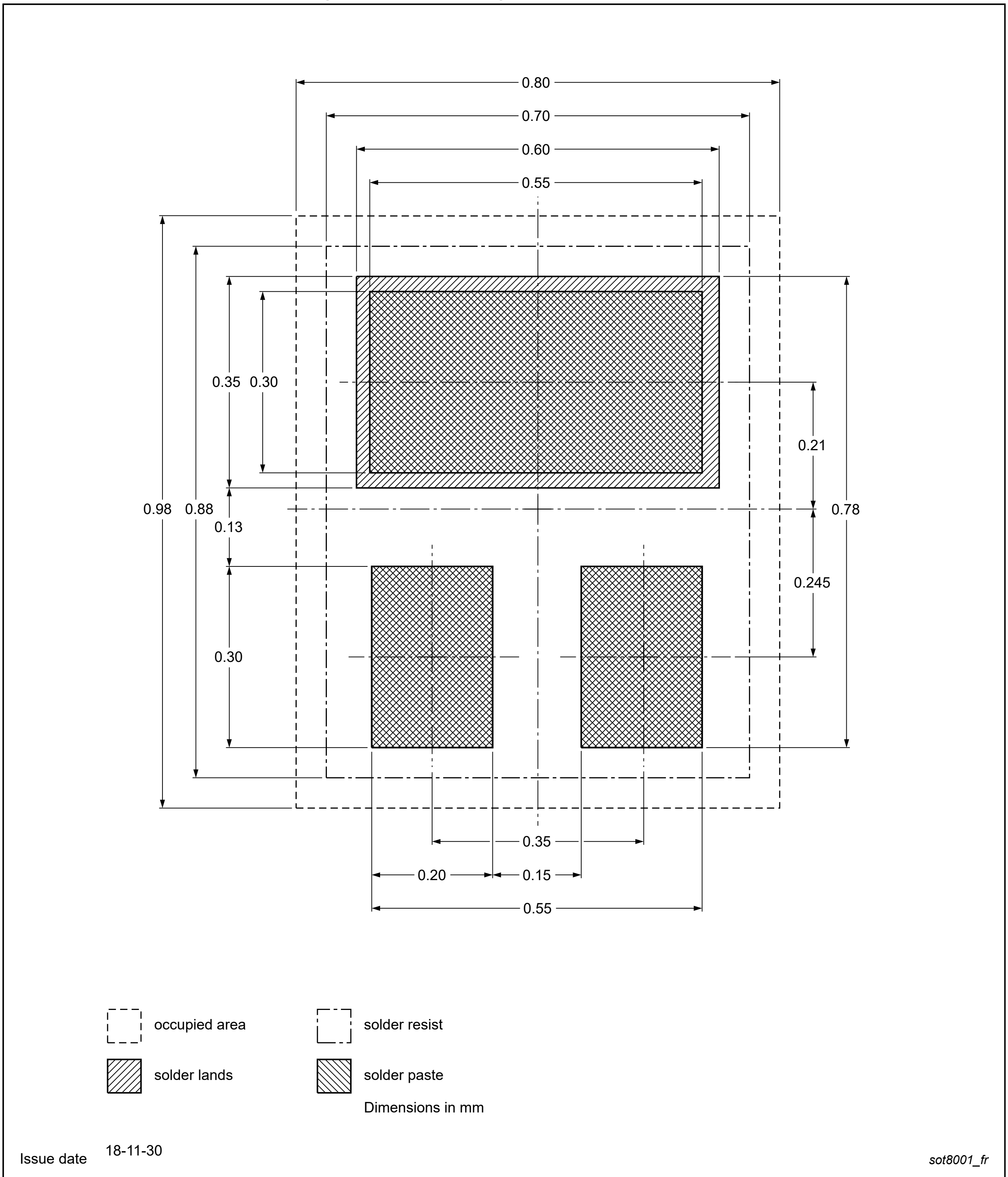


Fig. 20. Reflow soldering footprint for DFN0606-3 (SOT8001)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMH550UNEA v.1	20240711	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents

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